MLPF-WB and MLPF-NRG PCB design guidelines and reference hardware

Introduction

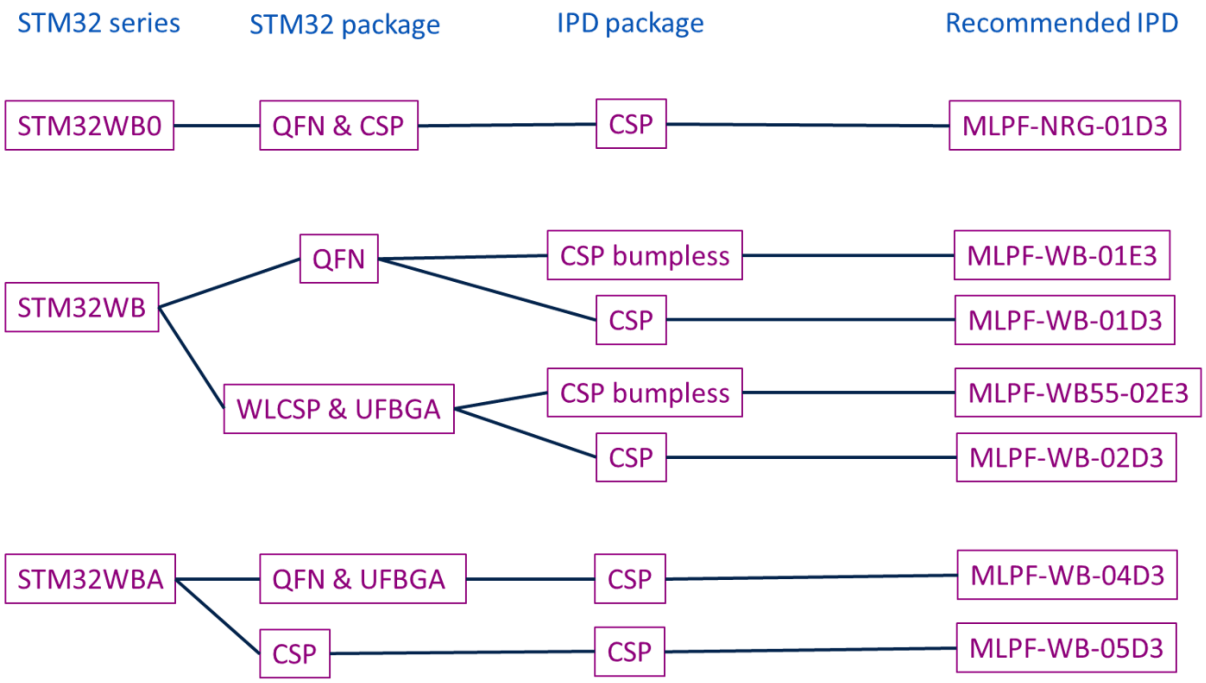
RF filters are critical components for wireless communication.

These filters ensure a robust and clean RF signal, enabling long-range and high-quality RF links.

To address this need, ST provides a comprehensive portfolio of companion chip filters specifically designed for each wireless STM32W microcontroller.

The Figure 1 presents the IPD filter selection tree based on the STM32 series, STM32 package, and IPD package.

Figure 1. IPD filter selection tree



The following pages provide the MLPF-WB and MLPF-NRG PCB design guidelines and reference hardware.

RF FILTER

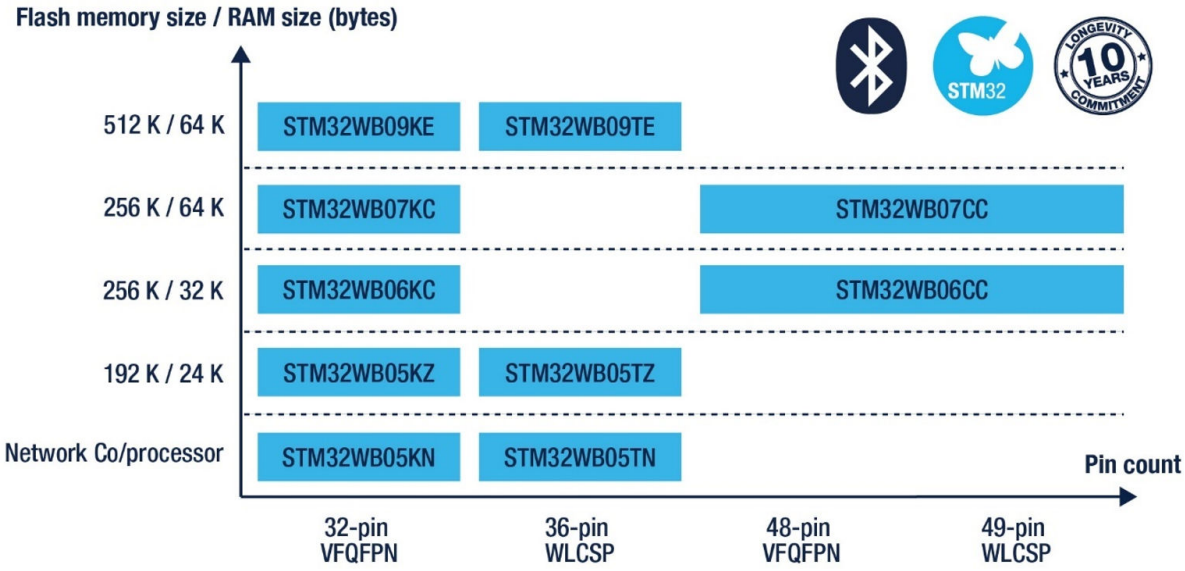
1 MLPF-NRG-01D3:

The STM32WB0 microcontroller series enables reliable wireless performance in a compact, energy-efficient design.

Based on the Arm Cortex®-M0+ core running at 64 MHz, the series offers up to 512 KB of flash memory and 64 KB of RAM.

Certified for Bluetooth® LE 5.4, the STM32WB0 achieves best-in-class power consumption, making it ideal for cost-sensitive and energy-sensitive wireless applications.

Figure 2. STM32WB0 microcontroller series

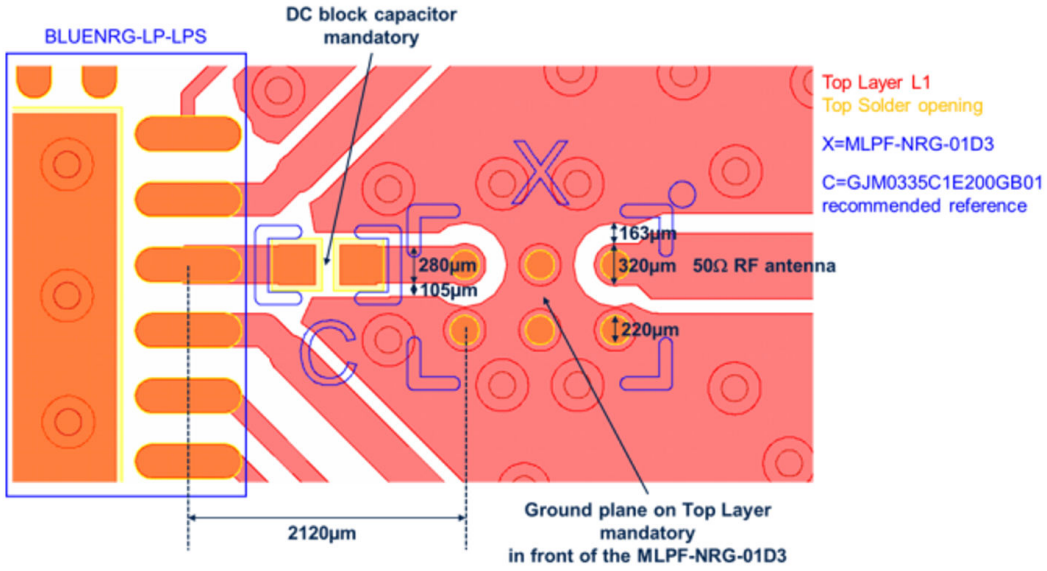


The MLPF-NRG-01D3 simplifies the implementation of the STM32WB0 series.

The MLPF-NRG-01D3 is compatible with the STM32WB0 in both QFN and CSP packages. It ensures compliance with all standard levels while providing proper impedance matching to maximize the output power level.

The MLPF-NRG-01D3 datasheet provides layout information, as shown in the Figure 3:

Figure 3. MLPF-NRG-01D3 layout



The transmission line between the MLPF and the antenna must have a 50 Ω characteristic impedance.

The transmission line between the STM32 and the MLPF must have a 57 Ω characteristic impedance.

Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

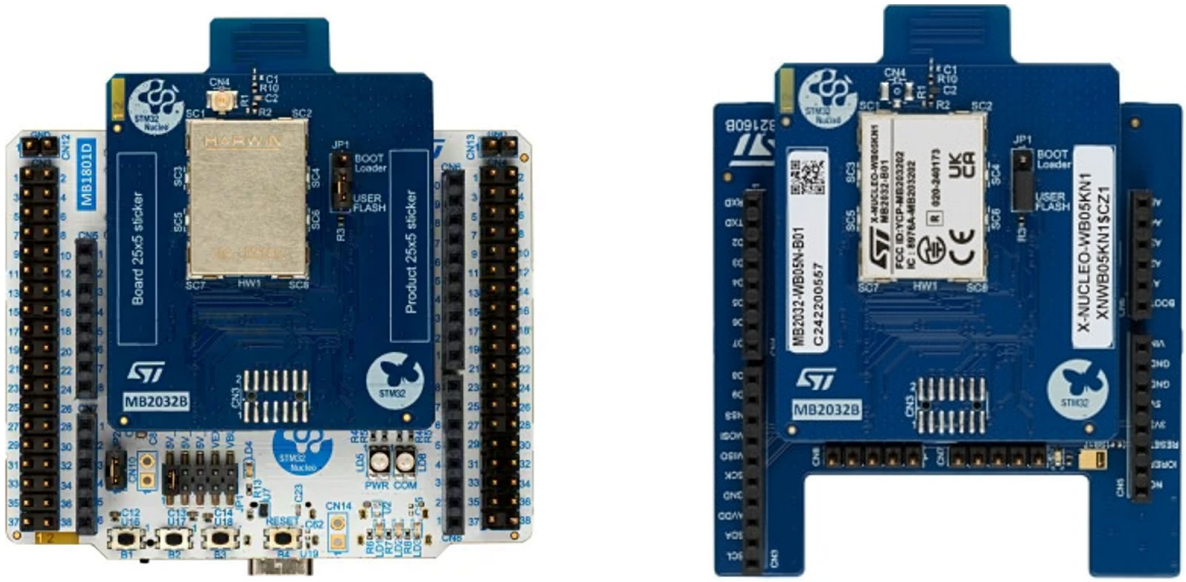
Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

The drill density must be maximized near the MLPF-NRG-01D3 area to ensure optimal RF performance.

From an assembly perspective, the solder mask-defined approach must be followed to ensure the correct assembly height.

Reference design resources for the MLPF-NRG-01D3 are available on www.st.com with the NUCLEO-WB09KE and X-NUCLEO-WB05KN1.

Figure 4. NUCLEO-WB09KE and X-NUCLEO-WB05KN1 views

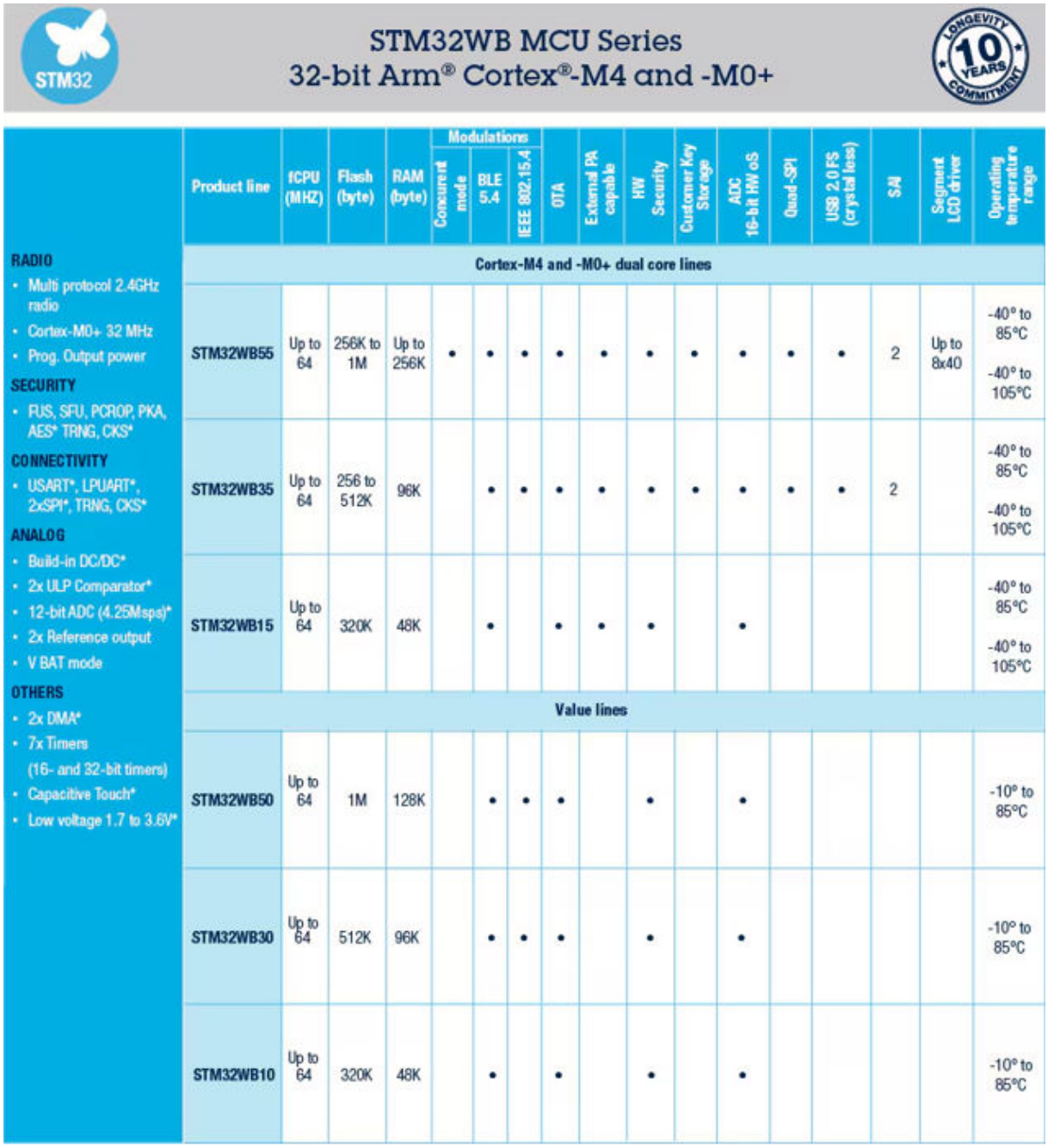


2 MLPF-WB-01E3:

STM32WB series is based on dual-core, multiprotocol wireless STM32WB microcontrollers that support Bluetooth® LE, Zigbee®, Thread®, and matter connectivity.

The STM32WB wireless microcontroller is a self-sufficient solution that integrates connectivity features and a general-purpose microcontroller in a single system-on-chip (SoC). It is based on an Arm Cortex®-M4 core running at 64 MHz (application processor) and an Arm Cortex®-M0+ core running at 32 MHz (network processor).

Figure 5. STM32WB MCU series



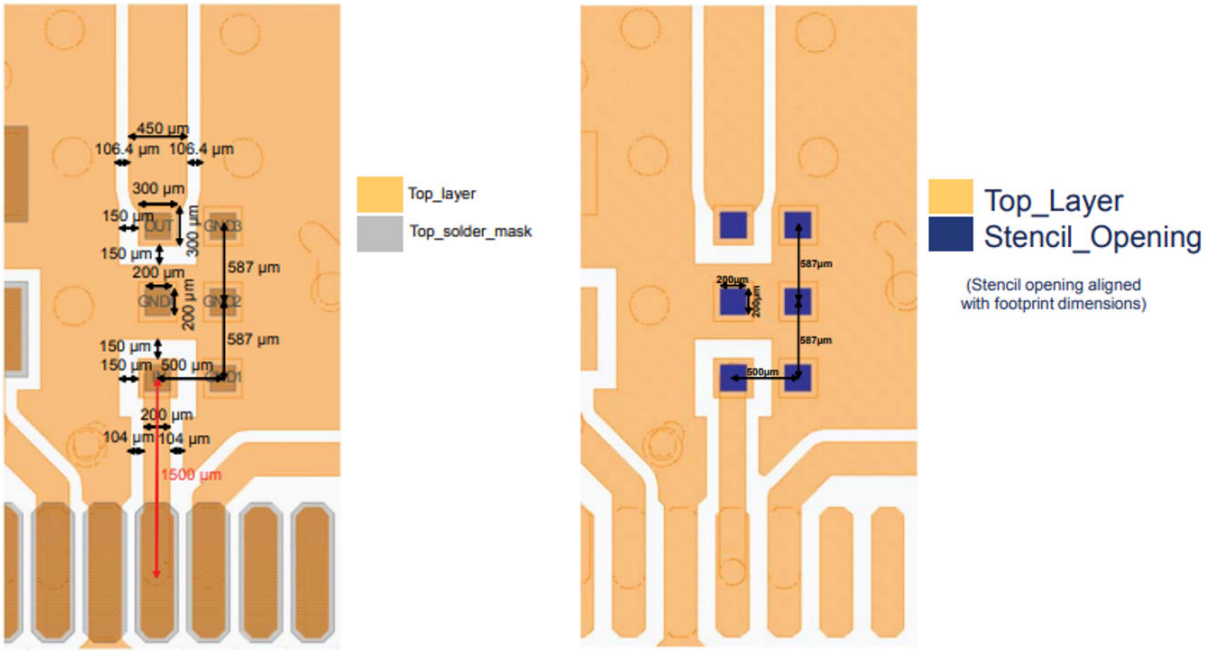
Product line	fCPU (MHz)	Flash (byte)	RAM (byte)	Modulations: Concurrent mode	Modulations: BLE 5.4	Modulations: IEEE 802.15.4	OTA	External PA capable	HW Security	Customer Key Storage	ADC 16-bit HW oS	Quad-SPI	USB 2.0 FS (crystal less)	S/W	Segment LCD driver	Operating temperature range
Cortex-M4 and -M0+ dual core lines																
STM32WB55	Up to 64	256K to 1M	Up to 256K	•	•	•	•	•	•	•	•	•	•	2	Up to 8x40	-40° to 85°C -40° to 105°C
STM32WB35	Up to 64	256 to 512K	96K		•	•	•	•	•	•	•	•	•	2		-40° to 85°C -40° to 105°C
STM32WB15	Up to 64	320K	48K		•		•	•	•		•					-40° to 85°C -40° to 105°C
Value lines																
STM32WB50	Up to 64	1M	128K		•	•	•		•		•					-10° to 85°C
STM32WB30	Up to 64	512K	96K		•	•	•		•		•					-10° to 85°C
STM32WB10	Up to 64	320K	48K		•		•		•		•					-10° to 85°C

The MLPF-WB-01E3 is compatible with the STM32WB series in the QFN package (for example, STM32WB55Cx, STM32WB55Rx, STM32WB50Cx, STM32WB35Cx, STM32WB30Cx). It ensures compliance with all standard levels and provides proper impedance matching to maximize the output power level.

The MLPF-WB-01E3 is a CSP bumpless component with an LGA footprint.

The MLPF-WB-01E3 datasheet provides layout information, as shown in the Figure 6 below:

Figure 6. MLPF-WB-01E3 layout



The transmission line between the MLPF and the antenna is designed for a 50 Ω characteristic impedance.

The transmission line between the STM32 and the MLPF is designed for a 62 Ω characteristic impedance.

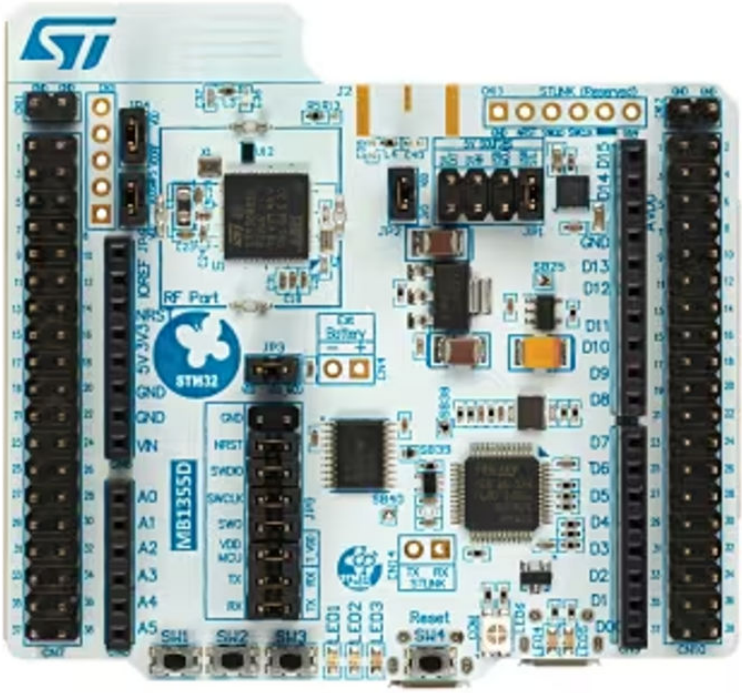
Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

From an assembly perspective, a solder mask-defined approach must be followed to ensure the correct assembly height.

Reference design resources for the MLPF-WB-01E3 are available on www.st.com with the NUCLEO-WB55RG.

Figure 7. **MLPF-WB-01E 3D view**



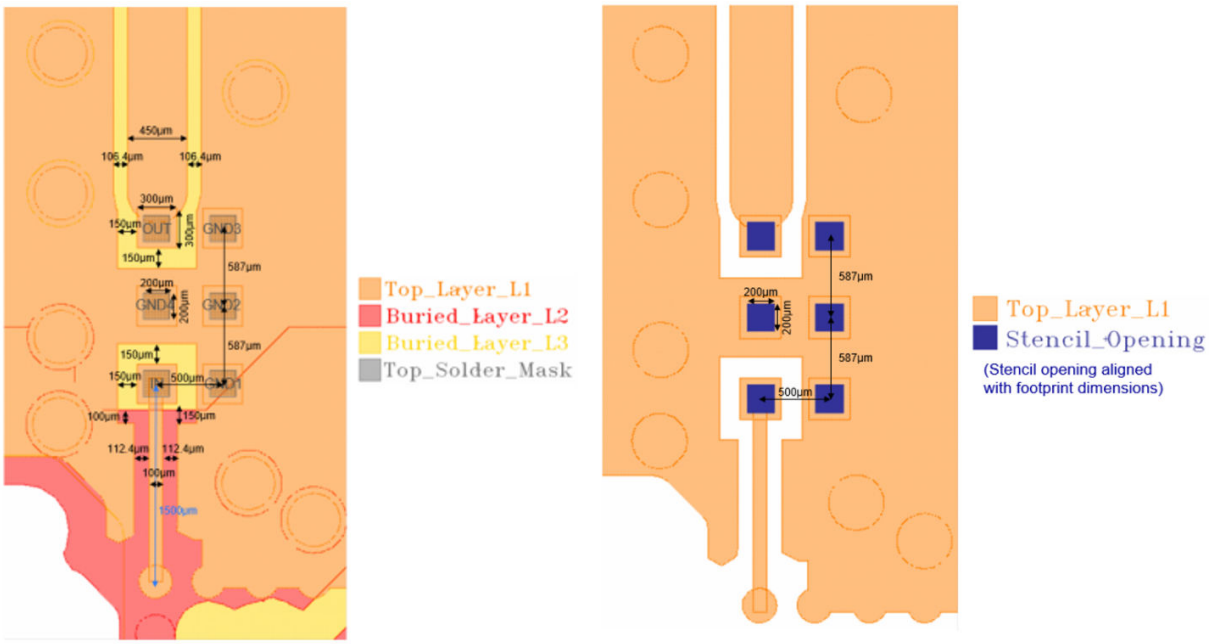
3 MLPF-WB55-02E3:

The MLPF-WB55-02E3 is compatible with the STM32WB series in WLCSP and UFBGA packages, such as STM32WB55Vx. It complies with all standard levels and ensures proper impedance matching to maximize the output power level.

The MLPF-WB55-02E3 is a CSP bumpless component with an LGA footprint.

The MLPF-WB55-02E3 datasheet provides layout information, as shown in the Figure 8 below:

Figure 8. MLPF-WB55-02E3 layout



The transmission line between the MLPF and the antenna is designed for a 50 Ω characteristic impedance.

The transmission line between the STM32 and the MLPF is designed for a 56 Ω characteristic impedance.

Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

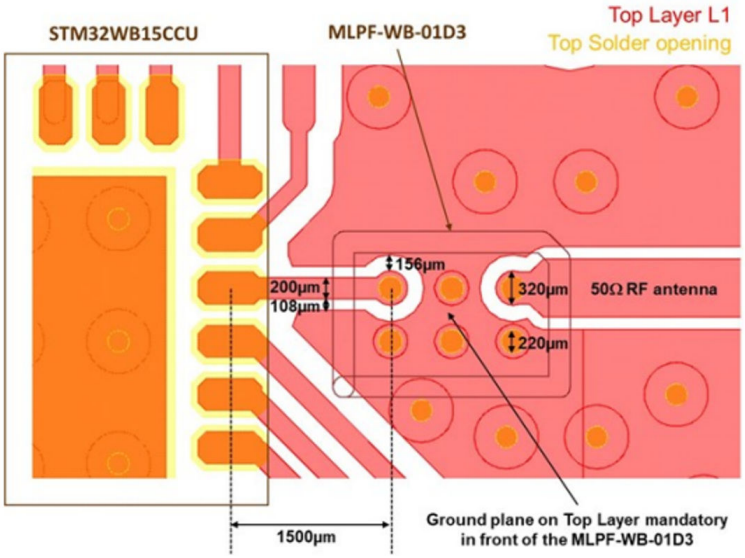
From an assembly perspective, the solder mask-defined approach must be followed to ensure the correct assembly height.

4 MLPF-WB-01D3:

The MLPF-WB-01D3 is compatible with the STM32WB series in UFQFPN and VFQFPN packages. It complies with all standard levels and provides proper impedance matching to maximize the output power level.

The MLPF-WB-01D3 datasheet provides layout information, as shown in the Figure 9 below. Refer to the datasheet at MLPF-WB-01D3.

Figure 9. MLPF-WB-01D3 layout



The transmission line between the MLPF and the antenna is designed for a 50 Ω characteristic impedance.

The transmission line between the STM32 and the MLPF is designed for a 67 Ω characteristic impedance.

Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

The drill density must be maximized near the MLPF-WB-01D3 area to ensure optimal RF performance.

From an assembly perspective, a solder mask-defined approach must be followed to ensure the correct assembly height.

Reference design resources for the MLPF-WB-01D3 are available on www.st.com for the MLPF-WB-01D3 with the NUCLEO-WB05KZ.

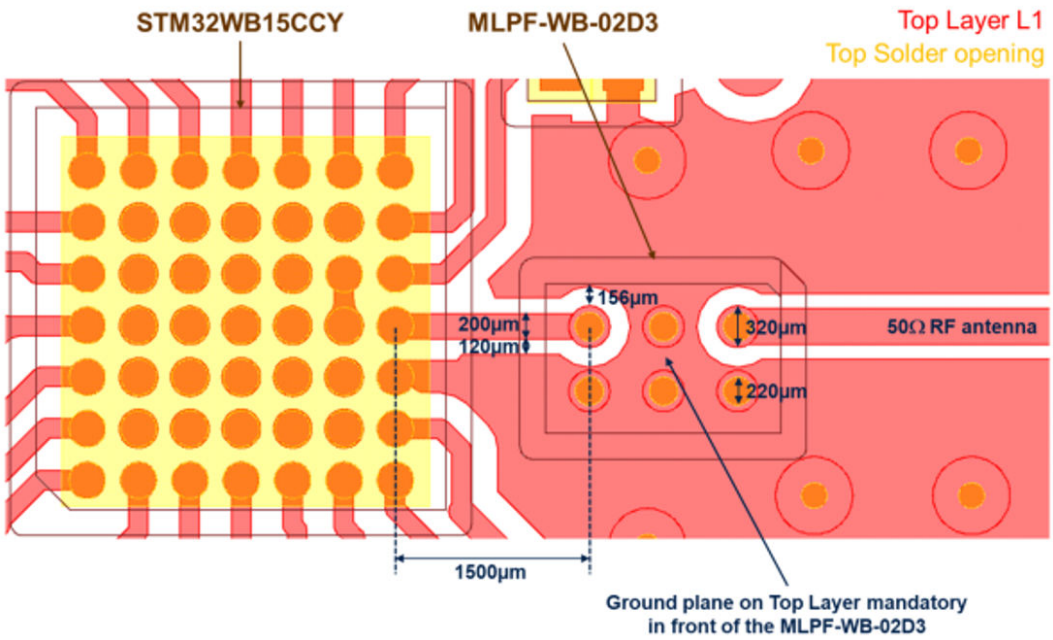
Figure 10. **MLPF-WB-01D3 3D view**

5 MLPF-WB-02D3:

The MLPF-WB-02D3 is compatible with the STM32WB series in WLCSP and UFBGA packages, such as STM32WB5x and STM32WB1x. It ensures compliance with all standard levels while providing proper impedance matching to maximize the output power level.

The MLPF-WB-02D3 datasheet includes layout information, as illustrated in the Figure 11 below:

Figure 11. MLPF-WB-02D3 layout



The transmission line between the MLPF and the antenna is designed for a 50 Ω characteristic impedance.

The transmission line between the STM32 and the MLPF is designed for a 61 Ω characteristic impedance.

Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

The drill density near the MLPF-WB-02D3 area must be maximized to ensure optimal RF performance.

From an assembly perspective, a solder mask-defined approach must be followed to ensure the correct assembly height.

6 MLPF-WB-04D3:

The STM32WBA MCU series offers designers performance, efficiency, and flexibility. It integrates large memory to support both applications and connectivity activities, featuring up to 2 Mbytes of flash memory and up to 512 Kbytes of RAM. A comprehensive set of peripherals, such as ADC, touch sensing, and timers, makes this product a self-sufficient wireless MCU for applications.

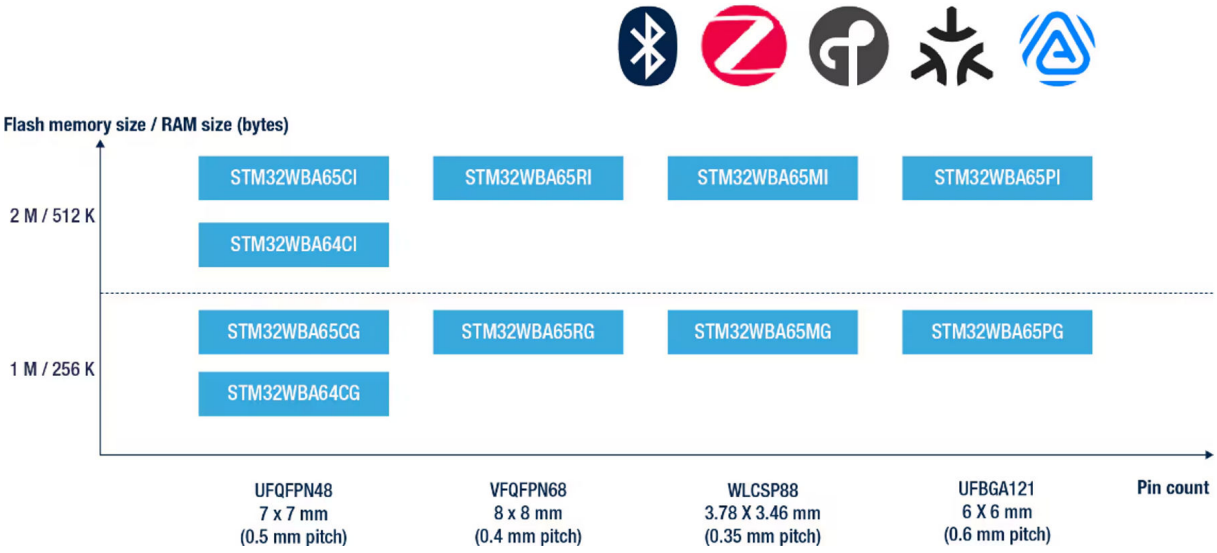
Key features include:

- High data rate: Ensures fast and reliable data transfer.
- Multiprotocol flexibility: Supports Bluetooth® LE 5.4, IEEE 802.15.4 communication protocols, Zigbee®, thread, and matter.
- Long-range capability: Extends communication range.
- High output power: Increases communication range with +10 dBm of output power.
- Low-power messaging capability: Extends battery lifetime.

Based on the Arm Cortex®-M33 core running at 100 MHz with TrustZone® technology, the STM32WBA series provides a high level of security, protecting data, intellectual property, and preventing hacks or device cloning.

Portfolio example of the STM32WBA65 family:

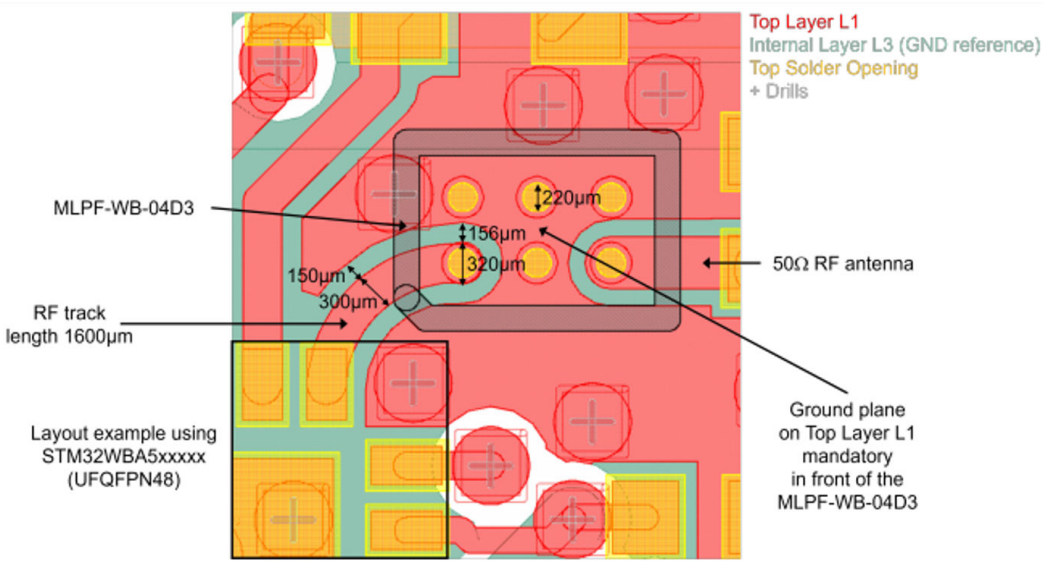
Figure 12. STM32WBA65 family



The MLPF-WB-04D3 has been developed to simplify the implementation of the STM32WBA series. It is compatible with STM32WBA in both QFN and BGA packages. The MLPF-WB-04D3 ensures compliance with all standard levels while providing proper impedance matching to maximize output power levels.

The MLPF-WB-04D3 datasheet provides layout information, as shown in the figure below:

Figure 13. **MLPF-WB-04D3 layout**



The RF transmission line between the MLPF and the antenna is designed for a 50 Ω characteristic impedance.

The RF transmission line between the STM32 and the MLPF is designed for a 63 Ω characteristic impedance.

Transmission line impedances and lengths must be precisely maintained. Adjust the physical line dimensions based on the actual PCB stack-up to ensure that the characteristic impedance aligns with the datasheet specifications.

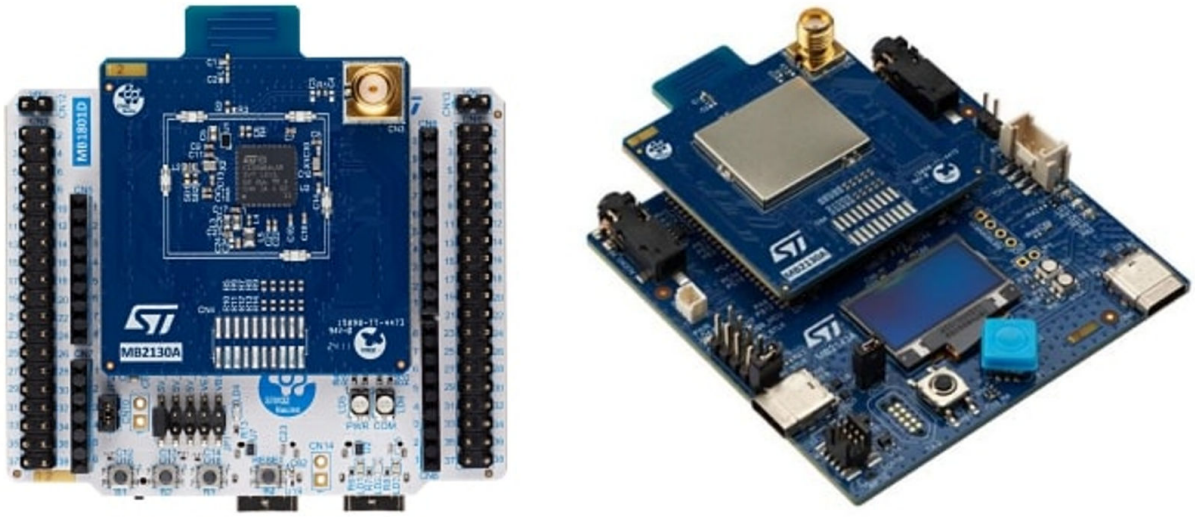
Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

The drill density near the MLPF-WB-04D3 area must be maximized to ensure optimal RF performance.

From an assembly perspective, a solder mask-defined approach must be followed to ensure the correct assembly height.

Reference design resources for the MLPF-WB-04D3 are available on www.st.com with NUCLEO-WBA65RI and STM32WBA65RI.

Figure 14. **3D view**

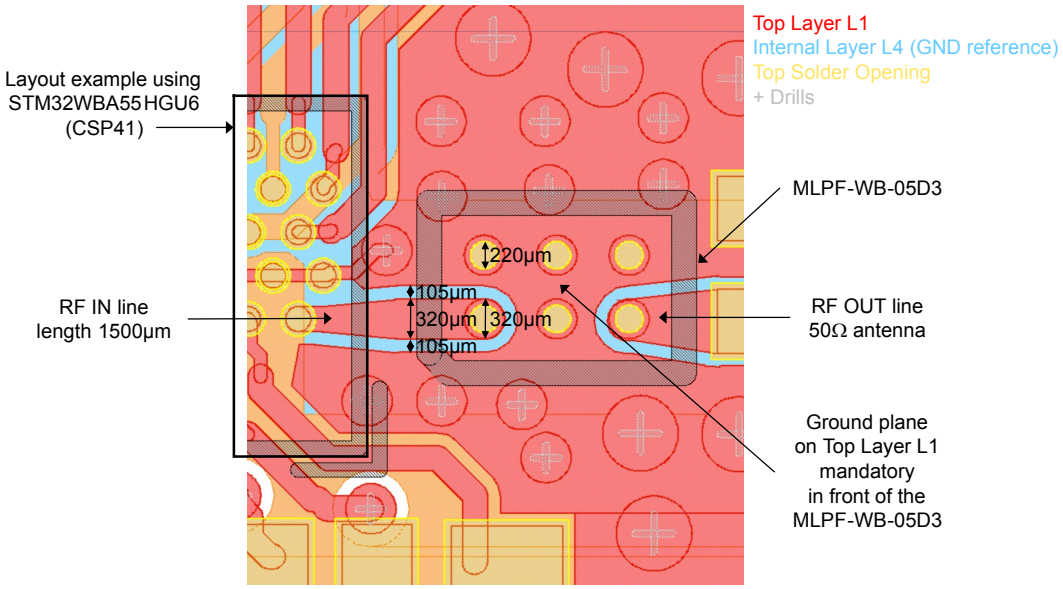


7 MLPF-WB-05D3:

The MLPF-WB-05D3 is compatible with STM32WBA in CSP package. It complies with all standard levels and provides proper impedance matching to maximize the output power level.

The MLPF-WB-05D3 datasheet includes layout information, as illustrated in the Figure 15 below:

Figure 15. MLPF-WB-05D3 layout



The RF IN transmission line between STM32 and MLPF is dimensioned to 55 Ω characteristic impedance.

This characteristic impedance has to be followed as close as possible, within a tolerance of ±15 %.

The length of the RF IN line must be followed as precisely as possible.

The RF OUT transmission line between MLPF and antenna is dimensioned to 50 Ω characteristic impedance.

The ground plane on top layer is mandatory in front of the MLPF-WB-05D3, with its geometries which allow the best equipotentiality.

The drill density near the MLPF-WB-05D3 area must be maximized to ensure optimal RF performance.

Special attention must be given to the clearance around the IN and OUT pads of the MLPF to achieve optimal RF performance.

From an assembly perspective, a solder mask-defined approach must be followed to ensure the correct assembly height.

Revision history

Table 1. **Document revision history**

Date	Revision	Changes
01-Aug-2025	1	Initial release.

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